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| EXAMINER |
|---|
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| 2614 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/191,629 | TRAN ET AL. | |
| | Examiner | Art Unit | |
| | Paulos M. Natnael | 2614 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-61 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-61 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims **1-5, 7, 34-37, 39** are rejected under 35 U.S.C. 102(e) as being anticipated by Swan, U.S. Pat. No. 6,304,297.

Considering claim **1**, Swan discloses all claimed subject matter, note;

a) the claimed method of storing incoming digital television data in the first frame buffer is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

b) the claimed method of reading outgoing digital television data from the second frame buffer is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

c) the claimed method of monitoring refresh of a display device coupled to the system is met by the disclosure that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23);

d) the claimed method of transmitting the outgoing digital television data in the second frame buffer to the display device when a programmed position of the display device is refreshed is met by the "display driver 16, which provides the display data 34 to a computer monitor or similar device" (col. 3, lines 15-16) and the disclosure that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23)

Considering claim **2**, Swan discloses all claimed subject matter, note;

a) the claimed method of storing the incoming digital television data in the second frame buffer is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

b) the claimed method of reading the outgoing digital television data from the first frame buffer is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

c) the claimed method of transmitting the outgoing digital television data in the first frame buffer to the display device when the programmed position of the display device is refreshed is met by the display driver 16 "which provides the display data 34 to a computer monitor or similar device" (col. 3, lines 15-16) and by the disclosure that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23)

Considering claim **3**, the claimed method of detecting whether the outgoing digital television data is stored in the first frame buffer or the second frame buffer is met by the disclosure that "the video processor 12 causes a frame, or field, of video data 28 to be stored in the back section 30 of frame buffer 14." (Col. 2, lines 66 to Col. 3, line 1)

Considering claim **4**, the claimed method of monitoring step comprising the step of monitoring a horizontal sync and a vertical sync of the display device, is inherent because, as Swan discloses, "....techniques have been developed to increase the synchronization between the display update rate of video images and the refresh rate of computer monitors." (Col. 1, lines 60-62)

Considering claim **5**, the claimed wherein the outgoing digital television data transmitted to the display device comprises a frame is inherent, because the data is written and read in frames by the frame buffers.

Considering claim **7**, the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data is met by the disclosure that "The display update rate 38 and the refresh rate 40 may be directly obtained from the video processor 12 and the display driver 16, respectively, or may be obtained by monitoring the read and write rate into and out of the frame buffer 14." (Col. 3, lines 64 to col. 4, line 1)

Considering claim **34**, Swan discloses all claimed subject matter, note;

a) the claimed first storing means for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

b) a second storing means for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

c) the claimed a monitoring means for monitoring refresh of a display device is met by video processor 12, Fig.1;

d) the claimed a transmitting means for transmitting the outgoing digital television data in a

storing means to the display device when a programmed position of the display device is refreshed, is met by the "display driver 16, which provides the display data 34 to a computer monitor or similar device" (col. 3, lines 15-16) and the disclosure that "...the display driver 16 is reading the data from the frame buffer 14 at the refresh rate and the video processor 12 is writing the data at the display update rate, where the display update rate and the refresh rate match." (Col. 3, lines 19-23

Considering claim **35**, a means for reading the outgoing digital television data from a storing means is met by display driver 16, which "is reading the data from the frame buffer 14..." (Col. 3, lines 16-17)

Considering claim 36, the claimed means for monitoring a horizontal sync and a vertical sync of the display

device.

Regarding claim 36, see rejection of claim 4.

Considering claim **37**, the claimed detecting means for detecting whether the outgoing digital television data is stored in the first storing means or the second storing means is met by video processor 12, FIG.1;

Considering claim 39, see rejection of claim 7.

3. Claims **57-61** are rejected under 35 U.S.C. 102(e) as being anticipated by Wilson et al. U.S. Pat. No. 6, 037,981.

Considering claim **57**, Wilson et al. discloses all claimed subject matter, note;

a) the claimed digital television/local bus interface logic for passing decoded digital television data First I/O bus 120, Fig.1;

b) the claimed a graphics controller for receiving the decoded digital television data over a local bus from the digital television/local bus interface logic is met graphics controller 113, FIG.1;

c) the claimed a display device for receiving the decoded digital television data from the graphics controller is met by the disclosure that "The graphics controller 113 interfaces to a display device (not shown in Fig.1) for displaying images rendered or otherwise processed by the graphics controller 113 to a user. Generally, the Display device may be a television set (analog or digital)...or other suitable display device. In embodiments of the present invention, the display device comprises a remotely located digital television [200, Fig.2]." (Col. 3, lines 65 to col. 4, lines 4)

Considering claim 58, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus is met by first and second I/O bus 112 and 120 respectively, or the processor bus 104, Fig.1;

Considering claim **59**, the claimed a core logic for receiving the decoded digital television data from the digital television/local bus interface logic and passing the decoded digital television data to the graphics controller is met by Bridge/memory controller 110, FIG.1, which "provides a graphics port (e.g. an Accelerated Graphics Port (AGP)) for connecting to a graphics controller 113." (Col. 3, lines 63-65).

Considering claim 60, the claimed digital television decoder for providing decoded digital television data to the digital television/local bus interface logic is met by the disclosure that "Digital television 200 comprises a receiver 202 for receiving the television signal to be converted into a picture for display to a user." (Col. 5, lines 57-59; see also col. 5, lines 30-56)

Considering claim 61, the claimed digital television tuner for providing encoded digital television data to the digital television decoder is met by the disclosure that "digital television 200 comprises a receiver 202 for receiving the television signal to be converted into a picture for display to a user."(Col. 5, lines 57-59; see also col. 5, lines 30-56)

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 8-33, 38, 48-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swan, U.S. Pat. No. 6,304,297 in view of the Admitted Prior Art (APA).

Considering claim 6, Swan discloses all claimed subject matter, except for;
The claimed method of transmitting the outgoing digital television data over a peripheral component interconnect (PCI) bus;

Regarding claim 6, Swan does not specifically disclose the PCI bus, however, Examiner takes Official Notice here in that the PCI bus connecting peripheral components or devices is well known in the art as the APA shows in FIG. 1 and therefore, would have been obvious to the skilled in the art.

Considering claim 8, Swan discloses all claimed subject matter, except for;

b) the claimed digital television/local bus interface logic coupled to the local bus is met by the video processor 12, Fig.1;

e) the claimed a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

f) the claimed second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

g) the claimed memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer is met by the video processor 12, FIG.1. (See also col. 2, lines 59-67)

Except for;

a) the claimed a local bus;

c) the claimed digital television interface for receiving incoming digital television data;

d) the claimed local bus interface for transmitting outgoing digital television data over the local bus;

Regarding a) and d), see rejection of claim 6.

Regarding c), Swan doesn't appear to disclose a separate interface unit for receiving incoming digital television data. Swan however discloses that "The video processing module 12 may include a television decoder, such that the video graphics circuit 10 may receive video data 26 from television broadcast, satellite broadcast, cable broadcast, DVD players, VCR players, etc." (See also col. 2, lines 61-65)

Therefore, it would have been obvious to the skilled in the art that the video processor 12 would perform the function of an interface to receive the incoming digital television data.

Considering claim 9, see rejection of claim 6.

Considering claim **10**, the claimed display device coupled to the local bus for receiving outgoing digital television data over the local bus is met by the disclosure that the "display driver 16 which provides display data 34 to a computer monitor or similar device";

Considering claim **11**, the claimed wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data

from the second frame buffer on a first portion of a refresh of a display device and transmits

the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device is met by the video processor 12, Fig. 1. (Col. 3, lines 1-4)

Considering claim **12**, the claimed wherein the memory controller stores the incoming digital television data to the second frame buffer and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device is inherent, because Swan teaches that "the frame buffer 14, by including a back section 30 and front section 32, is utilizing a technique known as double buffering [however] ***the frame buffer may include a single section***." (Col. 3, lines 4-11)

Considering claim 13, the claimed wherein the local bus interface monitors a refresh of a display device for receiving the outgoing digital television data is met by the video rate adjusting module 18, Fig. 1;

Considering claim **14**, the claimed wherein a refresh rate of the incoming digital television

data is decoupled from a refresh rate of the outgoing digital television data.

Regarding 14, see rejection of claim 7.

Considering claim **15**, the digital television local bus logic further comprising: *a write state machine* for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer.

Regarding claim 15, see rejection of claim 12.

Considering claim **16**, the claimed the digital television/local bus logic further comprising: *a read state machine* for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

Regarding claim 16, see rejection of claim 12.

Considering claim **17**, A digital television/local bus interface logic, comprising:

a) the claimed a digital television interface for receiving incoming digital television data is met by the video processor 12, Fig.1;

c) the claimed a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

d) the claimed a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

e) the claimed a memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer ***on a first portion of a refresh of a display device and transmitting the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device*** is met by the video processor 12, FIG.1. (See also col. 2, lines 59-67)

Except for;

b) the claimed a local bus interface for transmitting outgoing digital television data;

Regarding b), see rejection of claim 8 (c ).

Considering claim **18**, the claimed wherein the local bus interface comprises a peripheral component interconnect (PCI) interface.

Regarding claim 18, see rejection of claim 6.

Considering claim **19**, the claimed wherein the local bus interface transmits the outgoing digital television data over a local bus.

Regarding claim 19, see rejection of claim 6.

Considering claim **20**, see rejection of claim 11.

Considering claim **21**, see rejection of claim 12.

Considering claim **22**, see rejection of claim 14.

Considering claim **23**, see rejection of claim 15.

Considering claim **24**, see rejection of claim 16.

Considering claim **25**, Swan discloses the following claimed subject matter, note;

c) the claimed first buffer means for storing the incoming digital television data and the outgoing digital television data in an alternating manner is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

d) a second buffer means for storing the outgoing digital television data and the incoming digital television data in an alternating manner is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

e) the claimed controller means for storing the incoming digital television data to one buffer means and reading the outgoing digital television data from another buffer means is met by the video processor 12, FIG.1. (See also col. 2, lines 59-67)

Except for;

a) the claimed a first interface means for receiving incoming digital television data;

b)a second interface means for transmitting outgoing digital television data;

Regarding a) and b), Swan does not specifically disclose first and second interface means for receiving and transmitting tv data. However, Swan discloses the video processor 12 for receiving the video data 26 and display driver 16 for transmitting the display data 34 to a display device. (Fig.1) Besides, such interfaces are well known in the art. Therefore, it would have been obvious to the skilled in the art to recognize the teaching of the prior art and modify the system of Swan to provide separate interface means for receiving and transmitting television data.

Considering claim 26, the claimed wherein the second interface means for transmitting the outgoing digital television data comprises a peripheral component interconnect (PCI) interface.

Regarding claim 26, see rejection of claim 6.

Considering claim 27, see rejection of claim 6.

Considering claim 28, see rejection of claim 15.

Considering claim 29. see rejection of claim 16.

Considering claim 30, the claimed wherein the first interface means for receiving the incoming digital television data comprises a digital television interface.

Regarding claim 30, see rejection of claim 25 (a) and (b).

Considering claim 31, see rejection of claim 11.

Considering claim 32, see rejection of claim 12.

Considering claim 33, see rejection of claim 14.

Considering claim 38, see rejection of claim 6.

Considering claim 48, Swan discloses the following claimed subject matter, note;

d) the claimed first buffer means for storing the first incoming digital television data and the first outgoing digital television data in an alternating manner is met by the back section 30 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

e) a second buffer means for storing the first outgoing digital television data and the first incoming digital television data in an alternating manner is met by the front section 32 of frame buffer 14, Fig.1; (col. 3, lines 1-4 and col. 4, lines 32-35)

h) a memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital

television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of the refresh of the display device, transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device, and transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device is met by the video processor 12, FIG.1. (See also col. 2, lines 59-67)

Except for;

a) a first digital television interface for receiving a first incoming digital television data stream;

b) a second digital television interface for receiving a second incoming digital television data stream;

c) a local bus interface for transmitting a first outgoing digital data stream and a second outgoing digital television data stream;

f) a third frame buffer for storing the second incoming digital television data stream and the second outgoing digital television data stream in an alternating manner;

g) a fourth frame buffer for storing the second outgoing digital television data stream and the second incoming digital television data stream in an alternating manner;

Regarding (a) and (b), see rejection of claim 25 (a) and (b).

Regarding c), see rejection of claim 6.

Regarding f) and g), Swan discloses first and second sections of the frame buffer 14 utilized as first and second frame memories. Swan also however discloses that "As one of average skill in the art would readily appreciate, the frame buffer may include additional sections such that triple buffering or quadruple buffering techniques may be used." Therefore it would have been obvious to the skilled in the art to add two more section in order to make quadruple buffering and modify the system of Swan.

Considering claim 49, see rejection of claim 9.

Considering claim 50, the claimed wherein a refresh rate of the first outgoing digital television data stream is decoupled from a refresh rate of the first incoming digital television data stream and a refresh rate of the second outgoing digital television data stream is decoupled from a refresh rate of the second incoming digital television data stream is met by the disclosure that "The display update rate 38 and the refresh rate 40 may be directly obtained from the video processor 12 and the display driver 16, respectively, or may be obtained by monitoring the read and write rate into and out of the frame buffer 14." (Col. 3, lines 64 to col. 4, line 1)

Considering claim 51, see rejection of claim 9.

Considering claim 52, see rejection of claim 48 (d) and (e).

Considering claim **53**, Swan discloses the following claimed subject matter, note;

a) receiving encoded digital television data is met by video processor 12, Fig.1;

b) the claimed method of decoding the encoded digital television data to generate decoded digital television data is met by video processor 12, Fig.1, which "may include television decoder..." (Col. 2, lines 61-62)

Except for;

c) the claimed method of sending the decoded digital television data over a local bus of the computer system to a graphics controller;

Regarding c), Swan discloses video processor that may include a decoder to decode the received digital television data over a local bus. Swan doesn't specifically disclose a graphics controller; Swan discloses a video rate adjusting module 18 that receives an image content 36 from the video processor and processes the content sends a display update rate 42 to the processor. The APA discloses a graphics controller that, among other things, is used to process the refresh rate of the display screen.

Accordingly, therefore, it would have been obvious to one of ordinary skill in the art to replace the video rate adjusting module 18 in the system of Swan with graphics

controller of the APA in view of their closely related performance and the resulting expectation of similar output of refresh rate values of the display monitor or screen.

Considering claim 54, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus;

Regarding claim 54, see rejection of claim 6.

Considering claim 55, sending the decoded digital television data from the graphics controller to a display device.

Regarding claim 55, see rejection of claim 53 (c).

Considering claim 56, the claimed method of sending decoded digital television data over the local bus to core logic and from the core logic to the graphics controller.

Regarding claim 56, see rejection of claim 53 (c).

6. Claims 40-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drako et al., U.S. Pat. No. 5,451,981 in view of the Admitted Prior Art (APA).

Considering claim 40, Drako discloses the following claimed subject matter, note;

a) the claimed local bus is met by system bus 24, Fig. 4;

b)the claimed graphics controller coupled to the local bus is met control circuits 28, Fig.4;

c)the claimed display device for receiving outgoing digital television data from the graphics controller is met by display 27, Fig.4;

Except for;

d) the claimed digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed.

Regarding d), Drako doesn't specifically disclose digital television/local bus interface logic. However, Drako discloses a control circuit 31, Fig. 4. The Admitted Prior Art (FIG.1) discloses a TV tuner 18, graphics controller 14, core logic 10 and graphics controller frame buffer. Therefore, it would have been obvious to the skilled in the art to modify the system of Drako by adding the TV tuner and the core logic in order to provide outgoing digital television data (which the video input 30 would be capable of processing the television data with a simple modification of adding a TV tuner) over the local bus to the graphics controller when a programmed position of the display device is refreshed.

Considering claim 41, the claimed a core logic coupled between the local bus and the graphics controller.

Regarding claim 41, See rejection of claim 40.

Considering claim **42**, the claimed digital television decoder for providing incoming television data to the digital television/local bus interface logic;

Regarding claim 42, see rejection of claim 40.

Considering claim **43**, the claimed digital television tuner for providing incoming digital television data to the digital television decoder.

Regarding claim 43, see rejection of claim 40.

Considering claim **44**, wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether the programmed position of the display device is refreshed.

Regarding claim 44, see rejection of claim 40 (d).

Considering claim 45, the claimed wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device is inherent, because any video processing

system would have horizontal sync and vertical sync signal in order to properly function or operate.

Considering claim 46, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus.

Regarding claim 46, see rejection of claim 6.

Considering claim 47, the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding claim 47, see rejection of claim 14.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Broemmelsiek, U.S. Pat. No. 5574,836 discloses an interactive display apparatus and method with viewer position compensation comprising frame buffers and a graphics engine.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Paulos Natnael** whose telephone number is **(703) 305-0019.** The examiner can normally be reached on **Monday through Friday** from **5:30 a.m.** to **2:00 p.m.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John Miller**, can be reached on **(703)305-4795.**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is **(703)305-3900.**

***Any response to this action should be mailed to:***

Commissioner of Patents and Trademarks

Washington, D.C. 20231

***or faxed to:***

(703) 872-9314, (for formal communications intended for entry)

***or:***

(703)872-9314 (for informal or draft communications, please label "PROPOSED" OR "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, V.A. Sixth Floor (Receptionist).

***Paulos M. Natnael***

June 14, 2002

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600